



# SiI9125 HDMI Receiver with Deep Color Outputs

## Data Brief

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## Introduction

The SiI9125 HDMI Receiver with Deep Color Outputs is a second-generation dual-input High Definition Multimedia Interface (HDMI<sup>®</sup>), HDCP, and DVI compliant receiver. It is software-compatible with the SiI9133 receiver with Deep Color outputs as well as the SiI9033 receiver. Digital televisions that can display 10- or 12-bit color depth can now provide the highest quality protected digital audio and video over a single cable. The SiI9125 device can receive Deep Color video up to 12-bit, 1080p @ 60 Hz. Backward compatibility with the DVI 1.0 specification allows HDMI systems to connect to existing DVI 1.0 hosts, such as HD set-top boxes and PCs.

The latest generation Integrated Transition Minimized Differential Signaling<sup>™</sup> (TMDS<sup>™</sup>) core runs at 25–225 MHz and passes all HDMI compliance tests.

The SiI9125 receiver is pre-programmed with High-bandwidth Digital Content Protection (HDCP) keys and contains an integrated HDCP decryption engine for receiving protected audio and video content. This set of keys helps reduce programming overhead, lowers manufacturing costs, and provides the highest level of security.

The specialized audio and video processing contained in the receiver can add HDMI capability to earlier-generation consumer electronics. Efficient color space conversion receives RGB video data and delivers either standard-definition or high-definition YCbCr formats.

This receiver supports high end audio systems. An industry standard I<sup>2</sup>S port allows direct connection to low cost audio DACs at up to 192 kHz. Audio down-sampling allows the device to share the audio bus with a high-sample-rate audio DAC while down-sampling audio for an attached display supporting only lower rates. The device provides flexible power management.

## Digital Video Interface

- automatic video mode configuration simplifies firmware design
- 36-bit RGB/YCbCr 4:4:4
- 16/20/24-bit YCbCr 4:2:2
- 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
- 12/15/18-bit Digital Multimedia Output (DMO) RGB/YCbCr 4:4:4 (clocked with rising and falling edges)
- color space conversion for both RGB-to-YCbCr and YCbCr to RGB (both 601 and 709)
- true 12-bit accurate data using 14-bit processing

## Digital Audio Interface

- sends and receives 2-channel digital audio up to 192 KHz
- I<sup>2</sup>S output supports up to 2-channel 192 kHz digital audio
- The S/PDIF port supports 192 kHz compressed streams
- S/PDIF output supports PCM, Dolby Digital, and DTS
- IEC60958 or IEC61937 compatible
- 2:1 and 4:1 down-sampling to handle 96 kHz and 192 kHz audio streams

## Package

- 20 mm x 20 mm 144-pin TQFP package with an ePad<sup>™</sup>

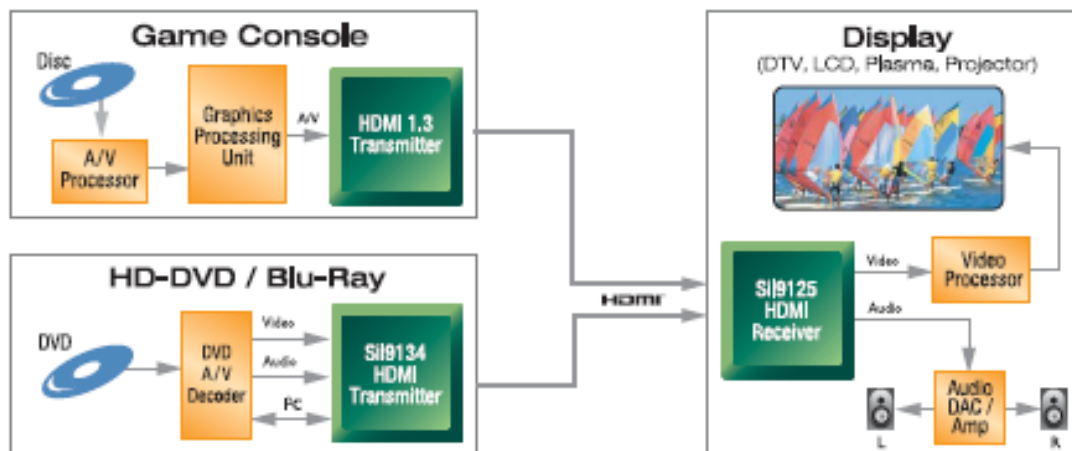


Figure 1. Typical Application

## Comparing SiI9125 with SiI9133 and SiI9023

Table 1 summarizes the functional differences among the SiI9023/9025, the SiI9133, and the SiI9125 receivers.

**Table 1. Summary of New Features**

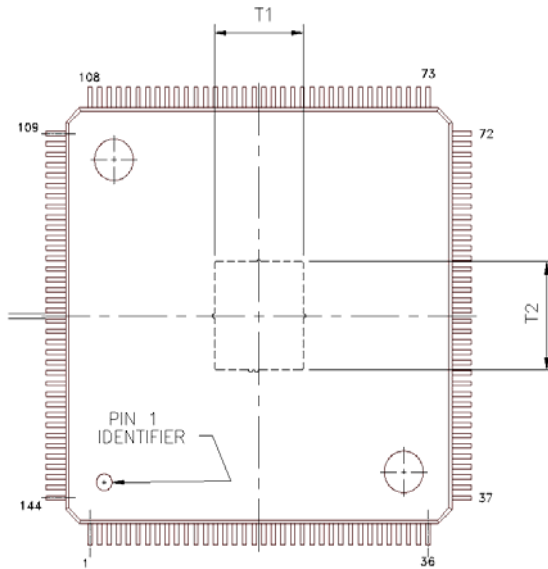
Feature	SiI9023/9025	SiI9133	SiI9125
<b>HDMI Input Connections</b>			
<b>TMDS Input Ports</b>	2	2	2
<b>Color Depth</b>	8-bit	8/10/12-bit	8/10/12-bit
<b>DDC Input Ports</b>	2	2	2
<b>Maximum TMDS Input Clock</b>	165 MHz	225 MHz	225 MHz
<b>Output Ports</b>			
<b>Digital Video Output Ports</b>	1	1	1
<b>Maximum Output Pixel Clock</b>	165 MHz.	165 MHz.	165 MHz.
<b>Maximum Output Bus Width</b>	24	36	36
<b>Analog Video Output Ports</b>	0	0	0
<b>S/PDIF Output Ports</b>	1	1	1
<b>I<sup>2</sup>S Output</b>	1	4	1
<b>Video Processing</b>			
<b>Color Space Converter</b>	RGB to/from YCbCr	RGB to/from YCbCr	RGB to/from YCbCr
<b>Pixel Clock Divider</b>	0.25, 0.5	0.25, 0.5	0.25, 0.5
<b>Digital Video Bus Mapping</b>	swap Cb, Cr pins	swap Cb, Cr pins	swap Cb, Cr pins
<b>Maximum Audio Sample Rate (Fs)</b>			
<b>2-channel (I<sup>2</sup>S or S/PDIF)</b>	192 kHz	192 kHz	192 kHz
<b>8-channel (I<sup>2</sup>S)</b>	N/A	192 kHz	N/A
<b>High Bit Rate Audio Support Compressed DTS-HD and Dolby True-HD</b>	No	No	No
<b>Other Features</b>			
<b>MCLK Generation</b>	No external connection required.	No external connection required.	No external connection required.
<b>HDCP Repeater Support</b>	No	Not Used	No
<b>Interlaced Format Detection Pin</b>	Yes	Yes	Yes
<b>TMDS R<sub>EXT_SWING</sub></b>	Not Used	Not Used	Not Used
<b>Package</b>	144-pin TQFP ePad	404-pin BGA w/Heat Slug	144-pin TQFP ePad



## Packaging

### ePad Enhancement

The SiI9125 receiver is packaged in a 144 pin TQFP package with an ePad™. The ePad dimensions are shown in Figure 3.



#### ePad Dimensions: Amkor and SPIL

Item	Description	Typ	Max
T1	ePad height	4.60	4.64
T2	ePad width	5.20	5.24

#### ePad Dimensions: ASE

Item	Description	Typ	Max
T1	ePad height	5.25	5.29
T2	ePad width	5.25	5.29

All dimensions are in millimeters.

The ePad is centered on the package center lines. The measurement tolerance is  $\pm 0.04$  mm for all manufacturers. The ePad tab dimensions may vary.

A clearance of at least 0.25 mm should be provided on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

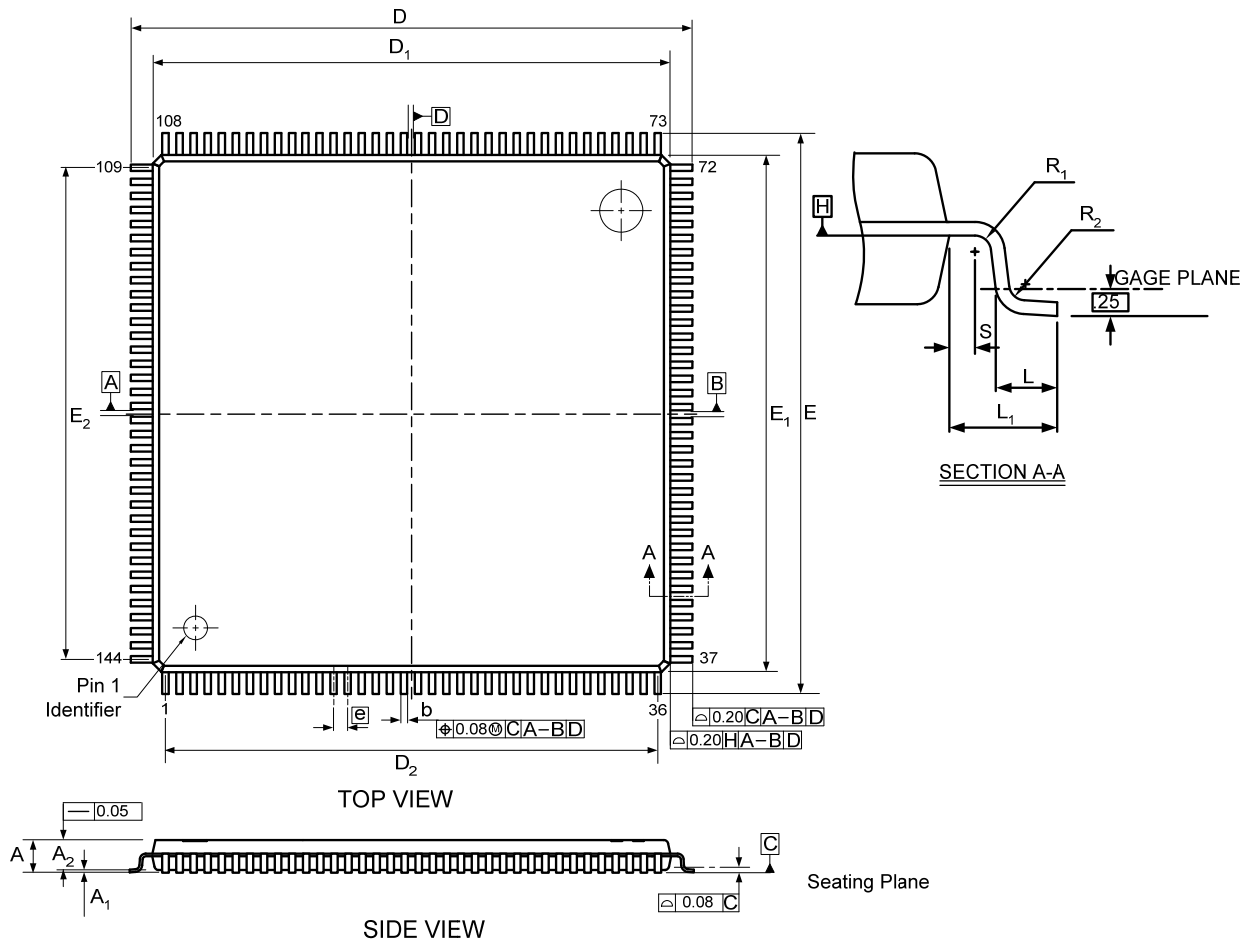
Silicon Image recommends that the ePad be soldered to the PCB and electrically grounded on the PCB. The ePad must not be connected to any other voltage level.

Figure 3. ePad Diagram

### PCB Layout Guidelines

PCB layout designers should refer to Silicon Image application note *PCB Layout Guidelines: Designing with Exposed Pads* (SiI-AN-0129) for basic design guidelines when designing with thermally enhanced packages using the Exposed Pad.

## Package Dimensions



JEDEC Package Code MS-026-AFB

Item	Description	Min	Typ	Max
A	Thickness	1.00	1.10	1.20
A1	Stand-off	0.05	0.10	0.15
A2	Body thickness	0.95	1.00	1.05
D	Footprint	22.00 BSC		
E	Footprint	22.00 BSC		
D <sub>1</sub>	Body size	20.00 BSC		
E <sub>1</sub>	Body size	20.00 BSC		
D <sub>2</sub>	Lead Row Width	17.5 BSC		
E <sub>2</sub>	Lead Row Width	17.5 BSC		

Item	Description	Min	Typ	Max
b	Lead width	0.17	0.22	0.27
C	Lead thickness	0.09	—	0.20
e	Lead pitch	0.50 BSC		
L	Lead foot length	0.45	0.60	0.75
L <sub>1</sub>	Total lead length	1.00 REF		
R <sub>1</sub>	Lead radius, inside	0.08	—	—
R <sub>2</sub>	Lead radius, outside	0.08	—	0.20
S	Lead horizontal run	0.20	—	—

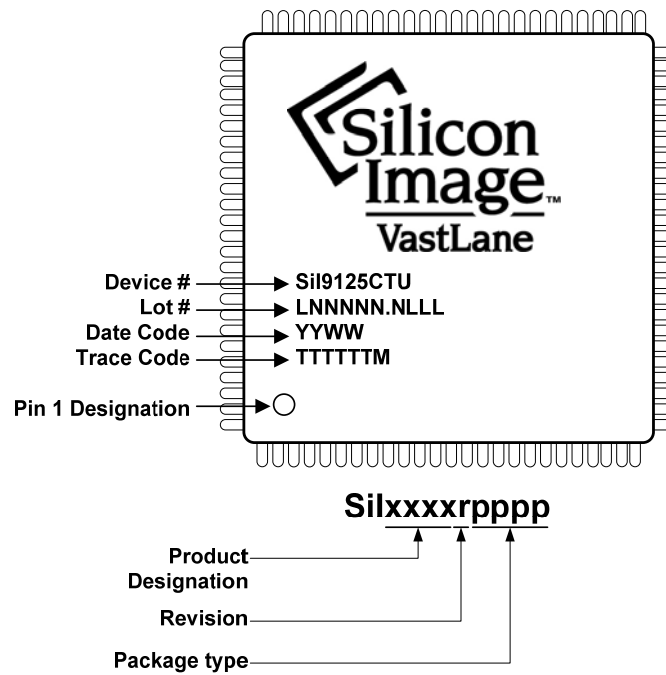
Dimensions in millimeters.

Overall thickness A = A<sub>1</sub> + A<sub>2</sub>.

Figure 4. Package Diagram

## Marking Specification

Drawing is not to scale and pin count shown is representative. Refer to specifics in [Figure 5](#) on page 5.



The universal package may be used in lead-free and ordinary process lines.

**Figure 5. Marking Diagram**

Legend	Description
LNNNNN.NLLL	Lot number
YY	Year of manufacture
WW	Week of manufacture
TTTTTT	Trace code
M	Maturity code

## Ordering Information

Production Part Numbers:

TMDS Input Clock Range	Part Number
25–225 MHz	SiI9125CTU



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